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REMARKS

Claims 1-5, 7-12, and 14-19 are pending in the application. By this Amendment, claims 2, 9 and 15 are amended, and claims 6 and 13 are canceled without prejudice or disclaimer to the subject matter set forth therein. Reconsideration and allowance in view of the foregoing amendments and following remarks are respectfully requested.

A. The 35 U.S.C. §112 Rejections

The Office Action rejects claims 2, 6, 9, 13, 15 and 19 under 35 U.S.C. §112, first and second paragraphs. The Office Action asserts various deficiencies regarding such claims. The claims have been amended in response to the asserted deficiencies.

However, Applicant requests the Examiner to reconsider the rejection of claim 19. The Office Action asserts that claim 19 recites the limitations, "the dual port memory", and "the setpoints" on page 13, line 20; and that there is insufficient antecedent basis for these limitations in the claim. However, based on Applicant's review of the claimed invention, it appears that there is antecedent basis for the recited terms so as to satisfy the requirements of 35 U.S.C. §112. The Examiner is respectfully requested to clarify or withdraw such grounds of rejection.

Applicant respectfully submits that the claims satisfy all requirements of 35 U.S.C. §112.

B. The Rejection of Claims 1, 8 and 15

The Office Action rejects claims 1, 8, and 15 under 35 U.S.C. 103(a) as being unpatentable over GFK-0728A (Programmable Controller IC697BEM763/764, 1 November 1995, hereinafter "GFK-0728A") in view of Kerr et al. (U.S. Patent Number 6,105,119, hereinafter "Kerr").

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The Office Action asserts that GFK-0728A discloses an interface module that interfaces between drive systems and local area network (LAN) protocols. The Office Action further discusses that GFK-0728A shows an interface between a drive and a LAN (Figure 2, on page 3, shows a labeled drawing of the module). The Office Action asserts although GFK-0728A shows substantial features of the claimed invention, GFK-0728A is silent as to the specific circuitry of the interface module; and that nonetheless the circuitry for interfacing a drive to a LAN is well known in the art and would have been an obvious modification to the system disclosed by GFK-0728A as evidenced by Kerr.

That is, the Office Action relies upon Kerr to allegedly cure the deficiencies of GFK0728A. The Office Action asserts that in analogous art, Kerr discloses data transfer circuitry that could be used to implement the system of GFK-0728A; and that in referring to claims 1, 8, and 15, Kerr shows, a dual port memory connected to a bus (column 3, lines 39-45, "Generally, and in one form of the present invention, an integrated circuit includes a dual-port memory having a first memory port and a second memory port, a bus interface block including bus master and bus slave circuitry, and a byte-channeling block coupled between the first memory port and the bus interface block operable to convert non-aligned data into aligned data.")

The Office Action further asserts that Kerr teaches an ASIC (column 3, lines 49-53, "The digital signal processor with an ASIC wrapper of this invention together provide super-bus-mastering to access the entire memory space in the system, including the entire virtual memory space accessible by the host processor."); an interrupt line (column 5, lines 51-53, "FIG. 28A is an electrical circuit diagram of interrupt-related registers and interrupt lines to the PCI bus and to

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the DSP, used in process, device and system embodiments"); and control registers (column 6, lines 17-21, "FIG. 38 is a DSP memory space diagram supplementing FIG. 36—right and showing DSP program, data and I/O spaces, including on-chip and off-chip memories and registers utilized in embodiments of processes, devices and systems herein").

Further, the Office Action asserts that given these teachings of Kerr, a person of ordinary skill in the art would have readily recognized the desirability and advantages of using the data transfer circuitry of Kerr to implement the system of GFK-0728A, in order to permit drives to be controlled from application programs.

Applicant traverses such assertions and the grounds of rejection set forth with respect to claim 1, for example. Claim 1 recites an interface card for interfacing a drive to a LAN without modifying a main control card of the drive, the interface card comprising a dual port memory interface to the main control card of the drive for receiving feedbacks and transmitting setpoints; an ASIC for generating an interrupt signal; an interrupt line that transmits the interrupt signal and informs a communication processor connected on the main control card to update the feedbacks in the dual port memory and read the setpoints from the dual port memory; and control registers for interfacing the communication processor to the LAN.

Accordingly, claim 1 relates to interfacing a drive to a LAN without modifying a main control card of the drive. In particular, the features of claim 1 relate to manipulation of feedbacks and setpoints. The applied art fails to teach or suggest such claimed features, including, for example, "an interrupt line that transmits the interrupt signal and informs a communication processor connected on the main control card to update the feedbacks in the dual port memory and read the setpoints from the dual port memory," as claimed.

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GFK0728A describes various features of a DLAN interface module. In particular, the GFK0728A document appears to focus on the protocols utilized, the physical arrangement of the modules, installation of the modules, and functions of the modules, for example. However, as acknowledged in the Office Action, GFK0728A fails to teach or suggest the particulars as recited in claim 1. Accordingly, the Office Action attempts to cure the deficiencies of GFK0728A with the teachings of Kerr.

Kerr is directed to data transfer circuitry, DSP wrapper circuitry and improved processor devices, methods and systems. In the Abstract, Kerr teaches an integrated circuit (1720) includes a dual-port memory (3330.1) having a first memory port (Port A) and a second memory port (Port B), a bus interface block (5010) including bus master (5016) and bus slave circuitry (5018), and a byte-channeling block (5310) coupled between the first memory port (Port A) and the bus interface block (5010) operable to convert non-aligned data addresses into aligned data. Kerr teaches a digital signal processor with an ASIC wrapper together provide super-bus-mastering to access the entire memory space in the system, including the entire virtual memory space accessible by the host processor.

In column 3, lines 25-36, Kerr describes further aspects including that hitherto, modem, voice, stereo audio, and other interfaces have often been implemented on respective add-in cards with respective software drivers and respective slave bus interfaces. Such system architecture has burdened OEM and business and consuming public with space requirements and financial expense. CPU MIPS are expended on the numerous slave transactions as well.

In column 13, lines 40-53, Kerr further describes that given an optimal way to deploy

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a "pool" of MIPS available in a computer system at any given time, a dynamically balanced system as described herein distributes and/or re-allocates its collective computational resources to satisfy a broad range of functional requirements on-the-fly. By comparison, a statically balanced system fails to perform some combinations of tasks even though there may be large "pools" of unused trapped MIPS in particular chip(s) in the system. Also, in column 15, lines 8-19, Kerr further describes in some of the embodiments herein called Unified Signal Processing (USP), the Windows OS is improved for OS directed device emulation, dynamic control, reconfiguration and allocation of system resources. Host emulation is augmented by distributed and asymmetrical device emulation acceleration. (Asymmetrical devices have different instruction sets or architecture.) Balanced system resources prevent or alleviate bus (CPU, memory and I/O) overloading, memory and I/O bottlenecks, and CPU stalls. By properly distributing computational resources in the system, device emulation tasks are directed by the OS to run on any appropriate processing elements to achieve balance.

Further, in column 16, lines 56-62, Kerr further describes a conventional x86 PC having a bursty bus such as PCI has multimedia performance improved by adding application specific integrated circuit (ASIC) "wrapper" circuitry to smooth out the data transfers into a desired stream-like flow of multimedia data. The data transfers are from host (system) memory to ASIC "wrapper" buffer memory for VSP consumption and vice versa. In column 20, lines 7-14, Kerr further describes time-slicing operating system code prevents an application from monopolizing the host by allotting runtime for the application in time slices thereby allowing other applications to be time-division-multiplexed. A preemptive

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multitasking OS further introduces a priority scheme to allow preemption of one task by another of a high priority. The improved USP system software granulates, or breaks up, applications into software objects called granules.

In column 134, lines 62-67, Kerr describes further aspects of the nature of the Kerr invention. Kerr describes a video input circuit receives video data from a video camera, video recorder, or camera-recorder (CAMERA) and supplies this data to system 100 for processing. A LAN (Local Area Network) circuit using TMS380 LAN and/or ThunderLAN(TM) technology from Texas Instruments provides two-way communication between system 100 and other computers having LAN circuits. Token ring, Ethernet, WAN and other advanced networks are accommodated.

Accordingly, set forth above, Applicant has set out various portions of the disclosure of Kerr so as to illustrate the nature of Kerr. It is respectfully submitted that based on the nature of Kerr, one would not have been motivated to combine the teachings of Kerr with GFK0728A. In short, Fig. 1 of Kerr relating to a TV tuner, a printer, 3D graphics and 3D audio appear reflective of the nature of Kerr. Such teachings of Kerr as described above, would not lead one of ordinary skill to utilize Kerr in GFK0728A, as proposed in the Office Action.

Further, the office action proposes the motivation that given the teachings of the applied art, a person of ordinary skill in the art would have readily recognized the desirability and advantages of using the data transfer circuitry of Kerr to implement the system of GFK-0728A, in order to permit drives to be controlled from application programs. However, it is submitted that it is not clear from the Office Action, what teachings of Kerr would be applied

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(and how it would be applied to GFK0728A) so as to allegedly allow drives to be controlled by an application program. The Examiner is requested to clarify this aspect of the rejection. That is, what aspect of GFK0728A is proposed to be modified by Kerr?

Further, even if it were obvious to somehow modify GFK0728A with the teachings of Kerr, which it is not, such would still fail to teach or suggest the features of claim 1. That is, claim 1 recites particulars related to the use of feedbacks and setpoints. The applied art fails to suggest such particulars, as claimed.

For example, Kerr describes that in FIG. 28A, interrupt-related registers and interrupt lines to the PCI bus and to the DSP, used in process, device and system embodiments have interrupts for PCI bus master 5016, DSP DMA SM 5030 interrupt, host-generated interrupt to DSP, stereo codec SM 5050 interrupt and voice code SM 5040 interrupt and host-generated NMI. Kerr teaches that these interrupts are supplied as indicated to the respective PCI interrupt register 2850 and DSP interrupt register 2860 as indicated in FIG. 28A, whereupon they are masked in the respective PCI interrupt mask register 2855 and DSP interrupt mask register 2865.

However, these teachings of Kerr fail to teach or suggest the claimed interrelationship between the interrupt line, the feedbacks, and the setpoints, for example, as recited in claim 1.

For at least the reasons set forth above. Applicant submits that the applied art fails to teach or suggest the claimed features, as recited in claim 1. Further, claims 8 and 15 define patentable subject matter for reasons similar to those set forth above with respect to claim 1. Withdrawal of the rejection under 35 U.S.C. §103 is respectfully requested.

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C. The Rejection of Claims 3-5 and 10-12

In the Office Action, claims 3-5 and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over **GFK0728A** in view of **Kerr** in further view of **GEI-100216** (Drive Control / LAN Communications Board DS200LDCC, May 1997, hereinafter "**GEI-100216**").

The Office Action describes that in referring to claims 3-6 and 10-13, although **GFK-0728A** in view of **Kerr** shows substantial features of the claimed invention, **GFK-0728A** in view of **Kerr** does not explicitly show a stab terminal, a LNPL connector, a 2PL connector or an AC/DC2000 drive; and that nonetheless these features are well known in the art and would have been obvious modifications to the system disclosed by **GFK-0728A** in view of **Kerr** as evidenced by **GEI-100216**.

Applicant submits that even if it were obvious to somehow combine the teachings of **GEI-100216** with the other applied art, **GEI-100216** would still fail to teach or suggest the features of claims 1 and 8 for the reason as set forth above.

Further, Applicant submits that the basis of the rejection is unsupportable and does not fairly teach or suggest the claimed invention. That is, Applicant submits that the Office Action is attempting to first modify **GFK0728A** with the teachings of **Kerr**, so as to allegedly teach the claimed circuitry, and then to modify such modified circuitry with the teachings of **GEI-100216**. Such attenuated modifications of the teachings of **GFK0728A** extend beyond what would have been obvious to one of ordinary skill in the art.

Accordingly, it is submitted that **GEI-100216** fails to cure the deficiencies of **GFK0728A** and **Kerr**, as discussed above. Dependent claims 3-5 and 10-12 define patentable subject matter for at least the reasons set forth with regard to the corresponding independent claims, as well as

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the additional features such dependent claims recite. Withdrawal of the rejection under 35 U.S.C. §103 is respectfully requested.

D. The Rejection of Claims 7 and 14

The Office Action rejects claims 7 and 14 under 35 U.S.C. 103(a) as being unpatentable over GFK-0728A in view of Kerr and in further view of GEH-6380 (Installation Guidance for Innovation Series Drive Systems, 30 June 1999, hereinafter "GEH-6380").

The Office Action describes that in referring to claims 7 and 14, although GFK-0728A in view of Kerr shows substantial features of the claimed invention, GFK-0728A in view of Kerr does not explicitly show the LAN is an ISBus LAN. Nonetheless this feature is well known in the art and would have been an obvious modification to the system disclosed by GFK-0728A in view of Kerr as evidenced by GEH-6380.

Accordingly, the Office Action attempts to combine GFK0728A and Kerr with the teachings of GEH-6380 so as to allegedly teach the claimed invention. However, Applicant submits that even if it were obvious to somehow combine the applied art, which it is not, the applied art would still fail to teach or suggest the features of claims 1 and 8, for the reasons set forth above.

That is, GEH-6380 fails to cure the deficiencies of the teachings of GFK0728A and Kerr. Dependent claims 7 and 14 define patentable subject matter for at least the reasons set forth with regard to the corresponding independent claims 1 and 8, as well as the additional features such dependent claims recite. Withdrawal of the rejection under 35 U.S.C. §103 is respectfully requested.

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E. The Rejection of Claims 16-19

The Office Action rejects claims 16-19 under 35 U.S.C. 103(a) as being unpatentable over **GFK-0728A** in view of **Kerr** in view of **Dye et al.** (U.S. Patent Number 6,523,102, hereinafter "**Dye**").

The Office Action reflects that in referring to claims 16-19, although **GFK-0728A** in view of **Kerr** shows substantial features of the claimed invention, **GFK-0728A** in view of **Kerr** does not explicitly show the steps of performing a page swap in memory after updating the feedbacks, storing the transmitted setpoints in an external RAM inactive page, and performing an external RAM page swap. The Office Action further asserts that nonetheless these steps are well known in the art and would have been an obvious modification to the system disclosed by **GFK-0728A** in view of **Kerr** as evidenced by **Dye**.

The Office Action asserts teachings of **Dye** related to using active and inactive pages of memory to store data, and swapping said memory to and from an active page to an inactive page (column 2, lines 61-67). The Office Action asserts that given the teachings of **Day**, a person of ordinary skill in the art would have readily recognized the desirability and advantages of modifying the system of **GFK-0728A** in view of **Kerr** so as to store memory in inactive and active pages, such as taught by **Dye**, in order to free memory that is no longer in use, to avoid over-committing the memory.

However, it is submitted that **GFK0728A** and **Kerr** fail to teach or suggest the claimed features relating to the manipulation of the feedbacks and setpoints as recited in claim 1 and discussed above; and that **Dye** fails to cure this deficiency with the asserted teachings relating to swapping, for example.

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Accordingly, it is submitted that claim 19 recites patentable subject matter for reasons similar to those discussed above with respect to claim 1.

Further, dependent claims 16-18 define patentable subject matter for at least the reasons set forth with regard to the claim 15, as well as the additional features such dependent claims recite. Withdrawal of the rejection under 35 U.S.C. §103 is respectfully requested.

F. Conclusion

For at least the reasons outlined above, Applicant respectfully asserts that the application is in condition for allowance. Favorable reconsideration and prompt allowance of the claims are respectfully solicited.

Should the Examiner believe anything further is desirable in order to place the application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

For any fees due in connection with filing this Response the Commissioner is hereby authorized to charge the undersigned's Deposit Account No. 50-0206.

Respectfully submitted,
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